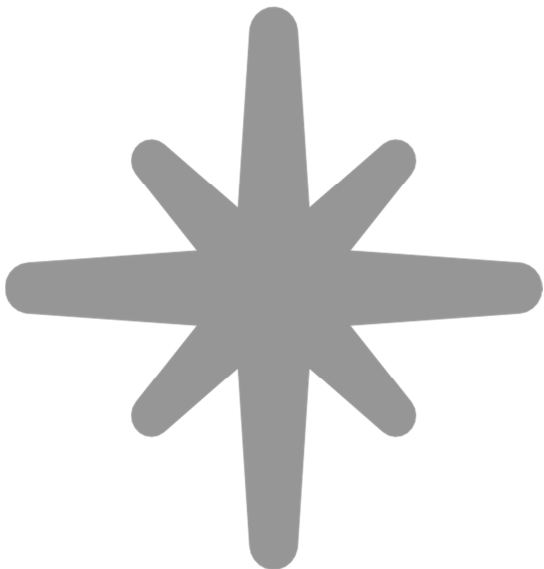


**GLYN**



**ATX-PRO  
Hardware &  
Software  
Manual**

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## Revision Table

Version	Date	Description
1	Nov 2011	Initial release for v3 hardware
2	March 2012	Updates for v3.1 hardware
3	May 2014	Updates for V5 hardware

## 1 ATX-PRO Hardware

The ATX-PRO board contains the following hardware and features:

- Atmel ATMega1280 embedded CPU.
- 128KB of external paged SRAM memory.
- Serial port dedicated to a GPS with a 1PPS signal and up to 10Hz cycle.
- Serial port dedicated to a Telit HSPA/GPRS CDMA, 3G, 4G modem module.
- Serial port dedicated to an Iridium satellite modem module, optional Wi-Fi and Bluetooth.
- Main RS232 serial port for connection to a PC or other serial device.
- Digital IO expansion interface including one NO/NC relay, 2 optically isolated outputs, 4 status LEDs and 8 bit digital IO bus configurable as A-D, digital inputs or outputs.
- Lithium ion polymer battery charger circuit.
- MicroSD card for non-volatile storage.
- 3 Axis Accelerometer.
- Battery backed up RTC.
- On board temperature sensor.

## 2 CPU Sub-System

The CPU on the ATX-PRO is an Atmel ATMega1280. Although this part is rated to 5V it operates at 3.4V to help conserve power consumption and so runs at a reduced speed of 11.0592MHz. This clock speed readily divides to support common standard serial port speeds.

### 2.1 RAM

The ATX-PRO contains a 128kB asynchronous SRAM device for RAM use in the range 0x2200 to 0xFFFF.

Internal RAM 0x0 - 0x21FF	External RAM Page 0 - A16=0 0x2200 - 0xFFFF
	External RAM Page 1 - A16=1 0x2200 - 0xFFFF

Although the ATMega1280 supports only 64kB of RAM total (internal and external) the external memory can be paged out using Port G Bit 4 to set or reset address bit A16. If the external memory is to be used in a paged fashion make sure that the stack, heap and other system RAM sections generated by the compiler all lie in internal memory below 0x2200 to avoid catastrophic system failure. Using paged memory is good for storing large amounts of logged data.

To enable external SRAM set registers XMCRA to 0x80 and XMCRB to 0x00.

See section 8 of the ATMega1280 Hardware Manual for more details on the external memory. Section 8.1.4 of the manual details how to utilize the normally unavailable first 8KB of external memory due to it being masked by the internal memory space. This will give a potential total of 136KB of RAM to use. The AVR-LIBC FAQ at:

<http://www.nongnu.org/avr-libc/user-manual/FAQ.html>

Details setting up the external memory registers as soon as the CPU comes out of reset.

The manual also has in:

[http://www.nongnu.org/avr-libc/user-manual/malloc.html#malloc\\_where](http://www.nongnu.org/avr-libc/user-manual/malloc.html#malloc_where)

a good discussion of allocating internal and external RAM with AVR-GCC.

## 2.2 Reset

There are several sources of external reset on the ATX-PRO. These are:

- U14 – MAX6326-R29 brown out reset detector
- J9 – ISP programming port
- J7 – JTAG port
- J6 – Serial port (for Arduino IDE compatibility)

The reset signal is active low. See chapter 11 of the ATmega1280 manual for more information on the reset behaviour of the CPU.

## 2.3 Power

The ATX-PRO has a sophisticated and flexible power supply system. The main supply is driven by an external source which can charge a local LiPo battery as well as power the board.

### 2.3.1 Main Supply

The primary power supply is connected to the 4pin Molex connector Pin 1 is the positive rail and pin 3 is the negative rail or ground reference. This supply is reverse polarity protected by D14 as well as fused on both the positive and negative rail to 4 amps each. For reliable operation the input supply voltage must be between +7V to +36V. **Do not exceed +36V.**

The primary supply is dropped to a system supply voltage of 4.2V from which all other on board voltages are derived.

### 2.3.2 GPS Supply

The GPS power supply is provided by a linear regulator to minimise power noise and maximise GPS sensitivity. CPU control of the supply is done by setting or clearing GPS\_3V3\_EN (P12) of U13.

A weak pull down on the control pin of the regulator will ensure the GPS is powered off while the CPU is in reset. Peak current available for the GPS modules is 150mA.

### 2.3.3 Expansion Port Power Supply

The expansion port P3 provides 4.2V for powering the optional daughter modules. CPU control of the supply is provided on the IO expansion chip U13 DT\_ONOFF (P14) and DT\_PWR\_CTRL (P13).

### 2.3.4 GSM Power Supply

The GSM/3G modem power supply is a filtered and controllable version of the primary +4.2V power supply. CPU control of the supply is done by setting or clearing P11 of U13. Once power is applied toggling Port L bit 0 will cause the modem to turn on and off internally. See the Telit hardware design manual for details on the toggling cycles. Reading Port E bit 3 will reflect the state of the power supply to the modem but functional testing by sending “AT<CR>” to the modem and getting an “OK” response back within about a second.

A weak pull down on the gate of the control FET Q4 will ensure the GSM/3G modem is powered off while the CPU is in reset. Resistor R143 will ensure the power to the modem is properly drained when switched off.

## 2.4 Battery Backup

### 2.4.1 Lithium Polymer Battery

The ATX-PRO can charge and be powered by a Lithium Polymer (LiPo) battery. An LTC4095 chip provides all the voltage and temperature monitoring and charging functions for the battery. The upper limit for charge current is set to 460mA. A discharged 3500mAh battery will therefore take almost 8 hours to charge.

Monitoring the battery state can be done by reading port L bit 5. The State this signal also directly drives LED D7. A steady high state means the battery is charging, a steady low(off) state means the battery is not or no longer charging(charge current has dropped to <10% of 460mA) and a blinking state means there is a battery or NTC fault. See the LT4095 manual on how to use the CPU to interpret the 2 blinking states.

Provision has been made to plug in two LiPo battery packs in parallel. Connector J3 is the primary battery connector and all single battery applications must use this connector. Use of J4 alone will cause the battery to discharge because the battery NTC is not connected to the charger on this port. The charger chip will not charge a lone battery only connected to J4 indicates a battery fault. The NTC on J4 is connected to ADC7 on the CPU instead.

## 2.4.2 RTC

The RTC (Real Time Clock) chip, need and use a battery backup to keep it running in a valid and useful state in the event there is no primary or LiPo battery power. The RTC needs to keep the time and date current. RTC chip using IIC to MCU, it connected to PD0 and PD1, and the IIC device address for this RTC chip is 0x6F.

## 2.5 Orderly Power Down

In the event that the ATX-PRO is shut down either by desire or the need avoid discharging the LiPo battery too deeply the following sequence should be used to power off the ATX-PRO to minimise any further power consumption.

- In the case of a low LiPo battery shut down is needed send an alert message back to base if possible.
- Save Iridium messages and other necessary state data to flash memory or the SD card.
- Cease any reads and writes to the SD card and any flash memory.
- GSM/Modem: Use the correct power off cycle on Port D bit 6 as indicated by the Telit manual. Monitor Port D pin 5 until it goes low meaning the modem is off.
- Shut down the power supplies to the GSM modem, GPS and Iridium modem.
- Set the accelerometer into standby mode and the temperature sensor into shut down mode.
- Turn off the relays, opto couplers and LEDs unless absolutely necessary – the relays drawn 50mA each when energised.
- Disable all interrupts including the watchdog, the 2 wire (I2C), external interrupts, and brownout.
- Set the CPU SM2:0 register to '010', set the SE bit to '1' and execute the SLEEP instruction to put the processor to sleep. The only way to way the CPU in this state is to provide a reset. Alternatively setting SM2:0 to '011' and execute the SLEEP instruction to put the CPU into power-save mode and use Timer 2 to occasionally wake the CPU to check the state of the battery or other stimulus to decide when to bring the CPU back into a fully operational mode.

## 2.6 Battery Charge Indicator

LED D7 reflects the state of the CHRG pin on U16. See the Linear LTC4095 data sheet for details.

- LED off: Battery is not charging
- LED on: Battery is charging
- LED dim then Bright: NTC or battery fault. The dim state is the signal being turned on and off at 35KHz. The duty cycle of the brightness indicates the particular fault.

This same signal can also be monitored by software on Port L bit 0.

## 3 CPU Ports

The following is an itemisation of the I/O port pins' utilisation on the ATmega 1280 along with recommended configuration values for the ATX-PRO.

As the CPU is operating at 3.4V the following input/output voltage levels to the port pins apply:

- $V_{IL}$ : 0V to 1.02V
- $V_{IH}$ : 2.04V to 3.4V
- $V_{OL}$ : 0 to 0.6V

V<sub>OH</sub>: 2.3 to 3.4V

### 3.1 Port A

Port Pin	Net Name	I/O	Description
PA7 - PA0	AD7 - AD0	X	Serves as multiplexed address and data bus (AD0-7) for external RAM.  Set whole port to TRISTATE  <b>PORTA = 0x00</b> <b>DDRA = 0x00</b>  (Note: External RAM must be configured first by setting <b>XMCR A = 0x80</b> and <b>XMCR B = 0x00</b> .)

### 3.2 Port B

Port Pin	Net Name	I/O	Description
PB7	PCINT7	I	optional for daughter board
PB6	DT_IO_1	I	Connected to daughter board
PB5	BAT_PWR	I	Battery power status. A '1' means the battery is powering the ATX-PRO, a '0' means the auxiliary power (plug pack or other source) is powering the ATX-PRO.
PB4	SD_IN	I	Micro SD plug unplug sense
PB3	MISO	I	SPI Master In Slave Out.
PB2	MOSI	O	SPI Master Out Slave In.
PB1	SCK	O	SPI Master/Slave Clock.
PB0	SD_CS	O	SPI Slave select, connected to daughter board extension connector

### 3.3 Port C

Port Pin	Net Name	I/O	Description
PC7 – PC0	A8 – A15	X	External SRAM address bits.  <b>PORTC = 0x00</b> <b>DDRC = 0x00</b>  (Note: External RAM must be configured by setting <b>XMCR A = 0x80</b> and <b>XMCR B = 0x00</b> .)



### 3.4 Port D

Port Pin	Net Name	I/O	Description
PD7	LED_R	O	Digital output. Red LED. '1' is on, '0' is off.
PD6	LED_O	O	Digital output. Orange LED. '1' is on, '0' is off.
PD5	LED_G	O	Digital output. Green LED. '1' is on, '0' is off.
PD4	LED_Y	O	Digital output. Yellow LED. '1' is on, '0' is off.
PD3	GSM_TXD_3V3	O	UART1 data transmit to GSM/3G modem.
PD2	GSM_RXD_3V3	I	UART1 data receive from GSM/3G modem.
PD1	SDA	I/O	Two Wire Interface (I <sup>2</sup> C) data pin.
PD0	SCL	I/O	Two Wire Interface (I <sup>2</sup> C) clock pin

### 3.5 Port E

Port Pin	Net Name	I/O	Description
PE7	GPS_1PPS_3V3	I	GPS 1PPS input
PE6	INT6	I	Connected to daughter board connector
PE5	DT_INT1	I	Connected to daughter board connector
PE4	IO_EXP_INT	I	IO expander interrupt input
PE3	PWR_MON_3V3	I	GSM/3G/4G modem power status input
PE2	PE2	I/O	Connected to daughter board connector
PE1	TX0	O	UART0 Transmit data to RS232 port.
PE0	RX0	I	UART0 Receive data from RS232 port.

### 3.5 Port F

Port Pin	Net Name	I/O	Description
PF7	ADC7 (TDI)	I	JTAG TDI. (Optional for the second battery NTC monitoring, need disable JATG to enable this ADC input)
PF6	ADC6 (TDO)	I	JTAG TDO.
PF5	ADC5 (TMS)	I	JTAG TMS.
PF4	ADC4 (TCK)	I	JTAG TCK.
PF3	ADC3	I	Connected to daughter board connector
PF2	DT_ADC_1	I	Connected to daughter board connector
PF1	VIN_ADC	I	External power supplier voltage monitoring, working as ADC

### 1.1

### 3.6 Port G

Port Pin	Net Name	I/O	Description
PG5	SD_CS	O	SD Card enable
PG4	A16	O	High address line of the external SRAM
PG3	CE	O	External SRAM chip enable. '0' enables SRAM, '1' disables.
PG2	ALE	O	SRAM address latch enable.
PG1	RD	O	SRAM read enable.
PG0	WR	O	SRAM write enable.  PORTG = 0x00 (Enable external SRAM, RLY1 NC) DDRG = 0b00111111 / 0x3F

### 3.7 Port H

Port Pin	Net Name	I/O	Description
PH7	FLASH_CS	O	External SPI flash chip select
PH6	DT_S_RTS	I/O	Connected to daughter board connector
PH5	DT_S_CTS	I/O	Connected to daughter board connector
PH4	DT_S_DCD	I/O	Connected to daughter board connector
PH3	DT_S_DSR	I/O	Connected to daughter board connector
PH2	DT_S_DTR	I/O	Connected to daughter board connector
PH1	GPS_RX_3V3	O	UART2 - GPS module data transmit (8N1 9600bps default)
PH0	GPS_TX_3V3	I	UART2 - GPS module data receive (8N1 9600bps default)  PORTH = 0x04 DDRH = 0b01100110 / 0x66  (note: UART2 must be enabled)

### 3.8 Port J

Port Pin	Net Name	I/O	Description
PJ7	DT_NET_AVA	I/O	Connected to daughter board connector
PJ6	ACC_INT1	I	Accelerometer interrupt1 input
PJ5	ACC_INT2	I	Accelerometer interrupt2 input
PJ4	RTC_INT	I	RTC interrupt input
PJ3	IGNITION_IN	I	Ignition input sense
PJ2	GSM_RING	I	RING signal for GSM modem. Use depends on the setting of the Telit modem's "IR" command.
PJ1	DTS TX	O	Connected to daughter board connector
PJ0	DTS RX	I	Connected to daughter board connector

### 3.9 Port K

Port Pin	Net Name	I/O	Description
PK7 - PK0	DIO_8 - DIO_1	IO	Configurable GPIO, Input, Output or ADC

### 3.10 Port L

Port Pin	Net Name	I/O	Description
PL7	GSM_DCD	I	DCD signal for GSM modem (Carrier Detect). Use depends on the setting of the Telit modem's "&C" command.
PL6	GSM_RTS	O	RTS signal for GSM modem (Ready to Send). Set to '0' means the modem can send data to the CPU. Set to '1' means the modem should

			stop sending data to the CPU. <i>It is strongly recommended that use of this pin is included in the serial port driver for UART1 to ensure no data is lost due to buffer overruns.</i>
PL5	CHARGE_STAT	I	Battery charge status signal from the LTC4095 charger chip.
PL4	GSM_DTR	O	DTR signal for GSM modem (Data Terminal Ready) Set to '0' means force the modem into command mode. Set to '1' means force the modem into transparent data mode.
PL3	GSM_CTS	I	CTS signal for GSM modem (Clear to Send) A '0' means the modem is ready to receive data. A '1' means stop sending any more data to the modem. <i>It is strongly recommended that use of this pin is included in the serial port driver for UART1 to ensure no data is lost due to buffer overruns.</i>
PL2	GSM_DSR	I	DSR signal for GSM modem (Data Set Ready) Use depends on the setting of the Telit modem's "&S" command.
PL1	STAT_LED_3V3R	I	GSM status indicator. This signal is normally used by the modem to drive a LED used to monitor the function state of the modem by observing the duty cycle of the signal. Read the Telit hardware manuals on the use of this pin.
PL0	GSM_OnOff	O	This is connected to a FET used to pull the GSM power activation line on and off. This is a toggling function. Read the Telit hardware manuals on the procedures and timing to toggle the modem on and off.

### 3.11 IO Expander

Port Pin	Net Name	I/O	Description
P17	OPMCU2	O	Output for Opto-coupler 2
P16	OPMCU1	O	Output for Opto-coupler 1.
P15	RELAY	O	Relay control
P14	DT_ONOFF	I/O	Connected to daughter board connector
P13	DT_PWR_CTRL	I/O	Connected to daughter board connector.
P12	GPS_3V3_EN	O	External GPS power control
P11	GSM_PWR	O	GSM/3G Modem power supply control
P10	GSM_RST_3V3	O	GSM/3G modem RESET
P07	DT_SUP_OUT	I/O	Connected to daughter board connector
P06	TMP75_INT	I	Temperature sensor interrupt
P05	DT_S_RI	I/O	Connected to daughter board connector
P04	TP10	I/O	Connected to test pad 10
P03	TP8	I/O	Connected to test pad 8
P02	HW_BIT2	I	
P01	HW_BIT1	I	
P00	HW_BIT0	I	

## 4 Interface Ports

### 4.1 CON1

#### 4.1.1 Connector

CON1 is a 30 pin connector that breaks out many of the signals on the ATX-PRO in order to provide scope to expand the application of the ATX-PRO with custom daughter cards and cable assemblies. Some of the signals routed to this connector are also routed to the CPU. The CPU can be disengaged from the nets by removing certain resistor and resistor block jumpers.

Note that some of the connections are directly connected to the GSM/3G modem and will require 1.8V or 2.6V CMOS logic levels. Check the relevant modem hardware manual for details.

Pin	Net Name	I/O	Description
1-2	4V2	PWR	This is a filtered and fuse protected version of the main power supply input. The supply can be in the range of 6V to 28V. This connection should only be ever used to source power to the ATX-PRO, not provide power. All external power should be sourced from connector P2.
3-4	GND	PWR	System ground.
5	DT_ONOFF	I/O	I/O from IO expander chip U13, P14
6	DTS_TX	O	UART 3 TX from MCU, PJ1
7	DTS_RX	I	UART 3 RX from MCU, PJ0
8	DT_PWR_CTRL	I/O	I/O from expander chip U13, P13
9	DTS_DCD	I/O	I/O from MCU, PH4
10	DTS_DSR	I/O	I/O from MCU, PH3
11	DTS_CTS	I/O	I/O from MCU, PH5
12	DTS_RI	I/O	I/O from expander chip U13, P05
13	DTS_RTS	I/O	I/O from MCU, PH6
14	DTS_DTR	I/O	I/O from MCU, PH2
15	GND	PWR	System Ground
16	SDA	I/O	IIC SDA from MCU, PD1
17	DT_NET_AVA	I/O	I/O from MCU, PJ7
18	SCL	I/O	IIC SCL from MCU, PD0
19	DT_INT_1	I/O	IO from MCU, PE5
20	DT_SUP_OUT	I/O	I/O from expander chip U13, P07
21	DT_ADC_1	I/O	IO from MCU, PF2
22	DT_IO_1	I/O	IO from MCU, PB6
23	EAR_HF+, DVI CLK	I/O	Hands free earphone positive signal. See Table 4 of UC864G hardware user guide. Digital Voice Interface clock signal for Telit modem.
24	SPI_CLK	I/O O	SPI Clock
25	EAR HF-, DVI TX	I/O	Hands free earphone negative signal. See Table 4 of UC864G hardware user guide. Digital Voice Interface transmit signal for Telit modem.
26	SPI_MOSI	I/O O	SPI Master Out Slave In
27	MIC HF+, DVI_RX	I/O	Hands-free microphone positive signal. See Table 1 of UC864G hardware user guide.

Pin	Net Name	I/O	Description
28	SPI_MISO	I	SPI Master In Slave Out
29	MIC HF-, DVI WA0		Hands-free microphone negative signal. See Table 1 of UC864G hardware user guide.
30	SPI_S_CS	O	SPI_CTRL signal.

## 4.2 P1

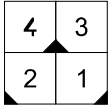
Microfit male 24 way connector – facing view.

24	23	22	21	20	19	18	17	16	15	14	13
12	11	10	9	8	7	6	5	4	3	2	1

Pin	Net Name	I/O	Description
1	V_IN		Alternative system supply input
2	Ignition	I	Ignition input, A voltage present on this pin will assert port PJ3 on the CPU. This will allow the CPU to recognise that a vehicle key is in the ignition position. V <sub>IL</sub> : 0V - 8V V <sub>IH</sub> : 9 - 36V
3	RL1_Com		Relay Common Pin (Omron G5V-1) V <sub>MAX</sub> 60VDC/125VAC I <sub>MAX</sub> 1A P <sub>MAX</sub> 30W/62.5VA
4	RL1_NC		Relay 1 Normally Closed Pin
5	Optional EXT_UART_RX	I	3V3 CMOS UART0 external interface receive optional
6	Optional EXT_UART_TX	O	3V3 CMOS UART0 external interface transmit optional
7	D_IO_p3	I/O	Protected Scaled Digital Input/Output Pull down jumper fitted: V <sub>IL</sub> : 0V-5V V <sub>IH</sub> : 7V-36V R <sub>IN</sub> : 14.5kΩ Pull down jumper not fitted: V <sub>IL</sub> : 0V-1V V <sub>IH</sub> : 2V-36V R <sub>IN</sub> : 110kΩ (Optional on hardware change to get extended input range; output with range 0 – 3.3V, current sensing, Analog input with configurable range)
8	D_IO_p2	I/O	Protected Scaled Digital Input/Output Pull down jumper fitted: V <sub>IL</sub> : 0V-5V V <sub>IH</sub> : 7V-36V R <sub>IN</sub> : 14.5kΩ Pull down jumper not fitted: V <sub>IL</sub> : 0V-1V V <sub>IH</sub> : 2V-36V R <sub>IN</sub> : 110kΩ (Optional on hardware change to get extended input range; output with range 0 – 3.3V, current sensing, Analog input with configurable range)
9	D_IO_p1	I/O	Protected Scaled Digital Input/Output Pull down jumper fitted: V <sub>IL</sub> : 0V-5V V <sub>IH</sub> : 7V-36V R <sub>IN</sub> : 14.5kΩ Pull down jumper not fitted: V <sub>IL</sub> : 0V-1V V <sub>IH</sub> : 2V-36V R <sub>IN</sub> : 110kΩ (Optional on hardware change to get extended input range; output with range 0 – 3.3V, current sensing, Analog input with configurable range)
10	PWR_GOOD Or External Battery	O	Depending on the fitting of J26 this pin can be configured to either indicate power good to an external lamp or be an alternative external battery supply for the system.
11	OP2	O	Optically isolated open collector output. (Sharp PC3H7) Absolute maximum collector current: 50mA Minimum V <sub>ce</sub> breakdown voltage: 70V Emitter connected to GND_1_2.
12	OP1	O	Optically isolated open collector output. (Sharp PC3H7) Absolute maximum collector current: 50mA Minimum V <sub>ce</sub> breakdown voltage: 70V Emitter connected to GND_1_2.
13	V_IN_GND		Complementary ground for V_IN
14	INHIBIT	I	Used in conjunction with R117 and R57 this pin should be connected to ground or earth (pin 4 on P2) when the battery or external supply is required to be disabled even if they are connected and available.
15	RL1_NO		Relay 1 Normally Open (Omron G5V-1) V <sub>MAX</sub> 60VDC/125VAC I <sub>MAX</sub> 1A P <sub>MAX</sub> 30W/62.5VA

16	3V PWR OUT		Option to provide 3V power to peripherals
17	D_IO_p8	I/O	Protected Scaled Digital Input/Output suitable for 1-Wire bus. This port is configured to drive a 1-Wire (iButton) bus. There is a pull up of 1.5k $\Omega$ to 3.3V to supply power to the 1-Wire devices. (Optional on hardware change to get extended input range; output with range 0 – 3.3V, current sensing, Analog input with configurable range)
18	D_IO_p7	I/O	Protected Scaled Digital Input/Output Pull down jumper fitted: $V_{IL}$ : 0V-5V $V_{IH}$ : 7V-36V $R_{IN}$ : 14.5k $\Omega$ Pull down jumper not fitted: $V_{IL}$ : 0V-1V $V_{IH}$ : 2V-36V $R_{IN}$ : 110k $\Omega$ (Optional on hardware change to get extended input range; output with range 0 – 3.3V, current sensing, Analog input with configurable range)
19	D_IO_p6	I/O	Protected Scaled Digital Input/Output Pull down jumper fitted: $V_{IL}$ : 0V-5V $V_{IH}$ : 7V-36V $R_{IN}$ : 14.5k $\Omega$ Pull down jumper not fitted: $V_{IL}$ : 0V-1V $V_{IH}$ : 2V-36V $R_{IN}$ : 110k $\Omega$ (Optional on hardware change to get extended input range; output with range 0 – 3.3V, current sensing, Analog input with configurable range)
20	D_IO_p5	I/O	Protected Scaled Digital Input/Output Pull down jumper fitted: $V_{IL}$ : 0V-5V $V_{IH}$ : 7V-36V $R_{IN}$ : 14.5k $\Omega$ Pull down jumper not fitted: $V_{IL}$ : 0V-1V $V_{IH}$ : 2V-36V $R_{IN}$ : 110k $\Omega$ (Optional on hardware change to get extended input range; output with range 0 – 3.3V, current sensing, Analog input with configurable range)
21	D_IO_p4	I/O	Protected Scaled Digital Input/Output Pull down jumper fitted: $V_{IL}$ : 0V-5V $V_{IH}$ : 7V-36V $R_{IN}$ : 14.5k $\Omega$ Pull down jumper not fitted: $V_{IL}$ : 0V-1V $V_{IH}$ : 2V-36V $R_{IN}$ : 110k $\Omega$ (Optional on hardware change to get extended input range; output with range 0 – 3.3V, current sensing, Analog input with configurable range)
22	GND		System ground
23	GND_2		Ground for Opto-coupler 2
24	GND_1		Ground for Opto-coupler 1

### 4.3 P2

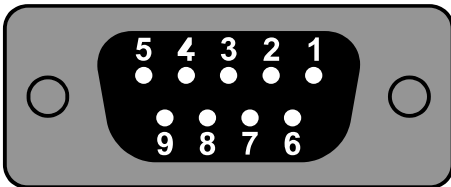


Microfit male

Pin	Net Name	I/O	Description
1	V_IN		System supply input. $V_{RANGE} +8V$ to $+28V$
2	Ignition		A voltage present on this pin will assert port PJ3 on the CPU. This will allow the CPU to recognise that a vehicle key is in the ignition position. $V_{IL}: 0V-1.1V$ $V_{IH}: 6.5V-40V$ $R_{IN}: 14.5k\Omega$ (Optional on hardware change to get extended input range; output with range 0 – 3.3V, current sensing, Analog input with configurable range)
3	V_IN_0V		System supply return or ground path.
4	Inhibit		Used in conjunction with R117 and R57 this pin should be connected to ground or earth (pin 4 on P2) when the battery or external supply is required to be disabled even if they are connected and available.

### 4.4 J6

Female DB-9 Connector.



Pin	Net Name	I/O	Description
1	4V2	-	This is a 4.2V direct connection (optional, not connected by default). Even though it is fused for 200mA be very careful with this pin. Do not connect it if it's not required.
2	RS232_TX	I	Data from DTE (PC) to DCE (ATX-PRO). This is the TX pin for a PC.
3	RS232_RX	O	Receive DCE (ATX-PRO) to DTE (PC). This is the RX pin for a PC.
4	RESET	I	This is the DTR signal on a PC. As per the Arduino usage of this pin, dropping the DTR signal from high to low will cause a short reset pulse to allow the ATX-PRO to reset. For Arduino users this will need the modified Arduino boot loader to be installed on the ATX-PRO. This reset will only work if J43 is closed.
5	GND	-	System Ground
6	NC	-	
7	NC	-	
8	NC	-	
9	NC	-	

### 4.5 U7/U15

Microfit male 6 way connector (facing view) and SIP header.





Pin	Net Name	I/O	Description
1	GPS_TXD	O	CPU to GPS serial data signal. Default 9600bps.
2	GPS_RXD	I	GPS to CPU serial data signals. Default 9600bps.
3	GND	-	
4	GPS_3V3	-	Power to GPS controlled by bit PE2.
5	GPS_VBAK	-	Battery backup power to GPS. This keeps the RAM state, clock and GPS almanac valid so the GPS can have a rapid reacquisition the next time it's powered up (the so called hot-start). If GPS_VBAK fails the GPS will be forced to take a long duration cold restart cycle.
6	GPS_1PPS	I	Provides a rising edge signal of 100ms duration that is aligned with the UTC second when the receiver has a valid 3D fix available.

#### 4.6 J3 and J4

Pin	Net Name	Description
1	4V2	4.2V LiPo battery rail.
2	BAT_NTC.	NTC temperature sensor inside the LiPo battery pack. On J3 this is connected to U16's NTC input. On J4 this is connected to ADC13 on the CPU.
3	GND	System ground.

#### 4.7 J9

This is the ISP header as used by AVR compatible FLASH programmers to rapidly configure the FUSE bits and access the EEPROM and FLASH memory on the Atmega1280.

Pin	Net Name	I/O	Description
1	MISO	O	Master In Slave Out
2	3V3	O	ISP Sense
3	SCK	I	ISP Clock
4	MOSI	I	Master Out Slave In
5	RESET	I	Reset
6	GND		System ground

#### 4.8 J7

This is the JTAG header as used by AVR compatible JTAG debuggers.

Pin	Net Name	I/O	Description
1	TCK	I	JTAG Test Clock
2	GND		System ground
3	TDO	O	JTAG Test Data Out
4	3V3	O	Sense voltage for JTAG debugger
5	TMS	I	JTAG Test Mode Select
6	RESET	I	JTAG Reset
7	3V3		Power for JTAG debugger. If the JTAG module needs power supplied by the

			ATX-PRO then J13 will need to be closed.
8	NC		
9	TDI	I	JTAG Test Data In
10	GND		System ground

## 5 Peripherals

### 5.1 GPS

The external GPS function is designed to fit a Fastrax UP501 family device either on board via the header on U15 or externally via the connector U7 with the UP501 “mouse”. Other makes and models may be used though so long as the can be powered by 4V and their serial and PPS I/O is compatible with 3.3V CMOS. If other voltages are needed reconfiguration of U3 will be required.

By default the UP501 emits many \$GPXXX messages every second but not all are necessary to acquire time and location. Most applications only need the \$GPRMC message for a time stamp and location fix. See the UP501 manual on how to enable and disable which the messages to be emitted. Minimising the amount of data coming from the GPS will keep the serial processing overhead down on the CPU.

To enable only the \$GPRMC message to be sent from the module the following command \$PMTK314,0,1,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0\* followed by the checksum.

The PPS (pulse per second) signal from the UP501 is available once a valid 2D fix is acquired. It's rising edge is at the top of the second (i.e. the instant the seconds value changes) and lasts for 100ms. This PPS signal can be used to align any internal clock that the application may have to UTC with an accuracy of 1us – but practically more like 1ms – to UTC. Relying on the serial messages alone will only give an accuracy of ±1 second. According to Fastrax the \$GPRMC message will always be emitted after the rising edge of the PPS.

### 5.2 GSM/3G Modem

The ATX-PRO can be fitted with a range of GSM and UMTS (3G) modems from Telit and supplied by Glyn that use the Molex #53949-0878 male 80 way connector. The modems feature a built in TCP/IP stack for IPv4 so that the ATX-PRO doesn't need to include its own TCP/IP stack. UDP and TCP are supported by these modems. If IPv6 is needed the ATX-PRO will have to support it with its own TCP/IP stack.

Some models such as the Telit UC864-G have a GPS function built in precluding the need to have a separate GPS module. The GPS function built into the modems doesn't have PPS output though so at best time synchronisation to UTC will be ±1 second using the \$GPRMC message.

The default data rate for most of the Telit modems is 115200bps but can be set higher. Hardware handshaking using CTS and RTS on the AVR must be used in the ATX-PRO serial port driver to avoid serial overruns and the resulting data corruption.

### 5.3 SBD9602/9603 Modem

The Iridium SBD9602/9603 modem can be fitted so the ATX-PRO can operate globally using the satellite based Iridium short message system. Hardware serial flow control (CTS and RTS) is disabled by default and isn't available to the ATX-PRO but shouldn't be needed due to the low data rates. Satellite Available line is available to alert the CPU of status changes to the modem.

### 5.4 MMA7455L Accelerometer

The MMA7455L Accelerometer is a 3 axis programmable range device that can measure acceleration peaks of 2G, 4G or 8G to 10 bit resolution. It is intended to operate off the I2C (or Two Wire Interface) bus built into the Atmega1280. The I2C address is 0x1D

Application notes AN3468 and AN3745 discuss the calibration procedures needed for the device along with application uses to detect freefall, shock and vibration. Port bits PJ5 and PJ6 on the CPU are hooked to the interrupt lines on the accelerometer to allow for rapid detection of adverse accelerations.

### 5.5 TMP75 Temperature Monitor

The temperature monitor is designed to record the ambient temperature of the ATX-PRO PCB. This device also sits on the I2C bus and has its address pins configured to have an I2C address of 0x4F. This too must be left

shifted once to set the address in the correct position.

Port bit P06 on the IO expander U13 is connected to the Alert signal on the TMP75 and can be used to alert the CPU if the temperature has fallen outside two programmable high and low temperatures.

## 5.6 SD Card

The SD card port can fit standard micro SD flash memory cards. The cards are accessed using the SPI port built into the Atmega1280. The user will need to supply a software stack that can handle any files systems on the card. MSDOS FAT16 and FAT32 formats are most commonly used but SD cards are not restricted to these two. Port bit PB4 on the CPU is connected to the card carrier to allow the CPU to detect whether or not a card has been fully inserted.

SD cards (indeed any flash based media) are prone to gross file system corruption or even catastrophic failure if the power being applied to them is interrupted in any way while they are writing to the flash memory cells. Cactus Technology do make an SD card that accommodates this and has enough power stored in an on-board capacitor to guarantee the completion of a write of the currently pending block (or sector) to flash memory if the main supply drops or glitches. This will prevent the card being corrupted and unusable but won't always stop a file system becoming inconsistent - but this depends entirely on the file system being used and it's resilience to interrupted writes. Many commercial grade SD cards will stop working at all if their power is interrupted during a write.

## 5.7 RTC

The RTC chip MCP7941 (U19) also sitting on IIC bus, its address is 0x6F, and is intended to allow the ATX-PRO to keep track of the current date and time even when the CPU is powered off or in a sleep mode.

Some Telit modems also have an RTC function built to them that can be used in conjunction with or in place of the MCP7941 but not all applications of the ATX-PRO will use a Telit modem.

## 6 Jumpers

Jumper	Description if Fitted
J13	This provides 3.3V to a JTAG device if the device needs to be powered by the ATX-PRO. Not all JTAG programmers need this power. Models with optical isolation or level shifting buffers usually require this jumper fitted.
J26	Setting the right and centre pad connects port P1 pin 5 to the positive rail of of the LiPo battery circuit to allow an external LiPo battery to be fitted. Setting the left and centre pad makes port P1 pin 5 available to drive a lamp or LED to indicate the status of U1 (the PG pin on the LT3690) that it is providing a regulated 4.5V supply to the ATX-PRO from an external source.
J43	If fitted this will allow the serial device on J6 to force a reset of the ATX-PRO. This is necessary for correct Arduino IDE operation (note that the Arduino boot loader will have to be installed on the CPU).

### 6.1 Web links

Here are web links to manufacturers of the devices used on the ATX-PRO. Direct links are not provided due to the ever changing nature of the vendors' websites.

The following peripherals can be purchased from the Glyn online store at <http://www.glynstore.com>.

ATX-PRO module: <http://www.glyn.com.au>

Telit GSM and UMTS modems: <http://www.telit.com>

Fastrax UP501 GPS modules: <http://www.fastraxgps.com>

Digi m10 Iridium modem: <http://www.digi.com>

Glyn also supply a range of suitable GPS, GSM, UMTS (3G) and Iridium antennas to suit your application.

Links to manufacturers of the other parts on the board:

AVR Atmega1280: <http://www.atmel.com>

TMP75 Temperature Sensor: <http://www.ti.com>  
MMA7455L Accelerometer: <http://www.freescale.com>  
All power supply chips: <http://www.linear.com>  
MCP7941 RTC: <http://www.microchip.com/>  
One-Wire Bus: <http://www.maxim-ic.com>

Other:

Industrial grade SD card: <http://www.cactus-tech.com>  
Iridium Network: <http://www.Iridium.com>  
SD Card Programming & Spec.: <http://www.sdcard.org>

## 7 Software Tools

### 7.1 Installing AVRStudio 4 and the GNU Tool Chain

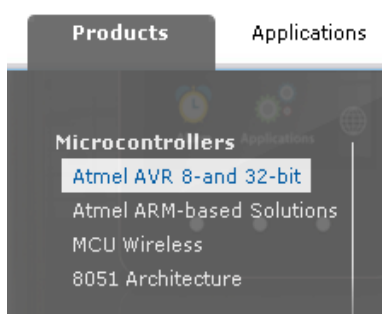
#### 7.1.1 Prerequisites:

- Windows 7 32 or 64 bit, Windows Vista or Windows XP. The installation procedures in this manual were developed using Windows 7 Home Edition 64 Bit.

AVRStudio 4 and the Atmel AVR GNU tool chain are the free Atmel supplied and supported IDE, assembler and C & C++ compiler for use with family of Atmel AVR microcontrollers. This document will guide the reader through the steps of downloading and installing the tool chain in preparation for starting to write code for the ATX-PRO development system.

#### 7.1.2 Downloading AVRStudio4 and AVRStudio6

- Using a web browser go to <http://www.atmel.com/>.
- Select Atmel AVR-8 and 32-bit from the Products menu then select “8 Bit MegaAVR”.



- Click on the Tools tab:



- Select AVRStudio4



- Scroll down to AVR Studio 4.19 (build 730) and click on the disk icon to register and download the installer.

The direct path to download this file is

[http://www.atmel.com/dyn/resources/prod\\_documents/AvrStudio4Setup.exe](http://www.atmel.com/dyn/resources/prod_documents/AvrStudio4Setup.exe)

- Back in the AVRStudio 4 section scroll down to the Atmel AVR Toolchain 3.3.0 for Windows and click on the disk icon to register and download the installer.

The direct path to download this file is

[http://www.atmel.com/dyn/resources/prod\\_documents/avr-toolchain-installer-3.3.0.710-win32.win32.x86.exe](http://www.atmel.com/dyn/resources/prod_documents/avr-toolchain-installer-3.3.0.710-win32.win32.x86.exe)

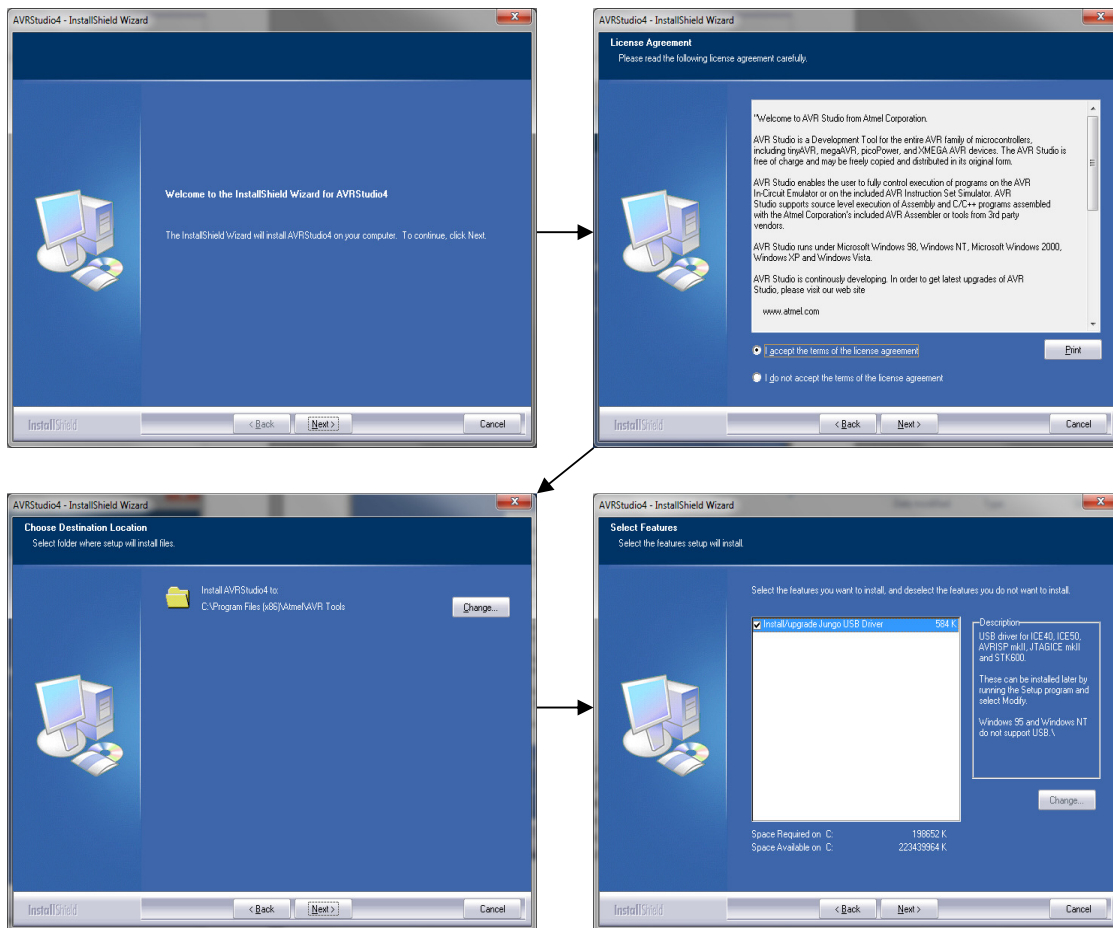
- Back in the Tools tab select Atmel AVR Studio 5.1. Scroll down to the AVR Studio 5 Installer – Full and click on the disk icon to register and download.

The direct path to download this file is:

<http://www.atmel.com/Images/as5installer-stable-5.1.208-full.exe>

#### 7.1.3 Installing AVRStudio 4.19

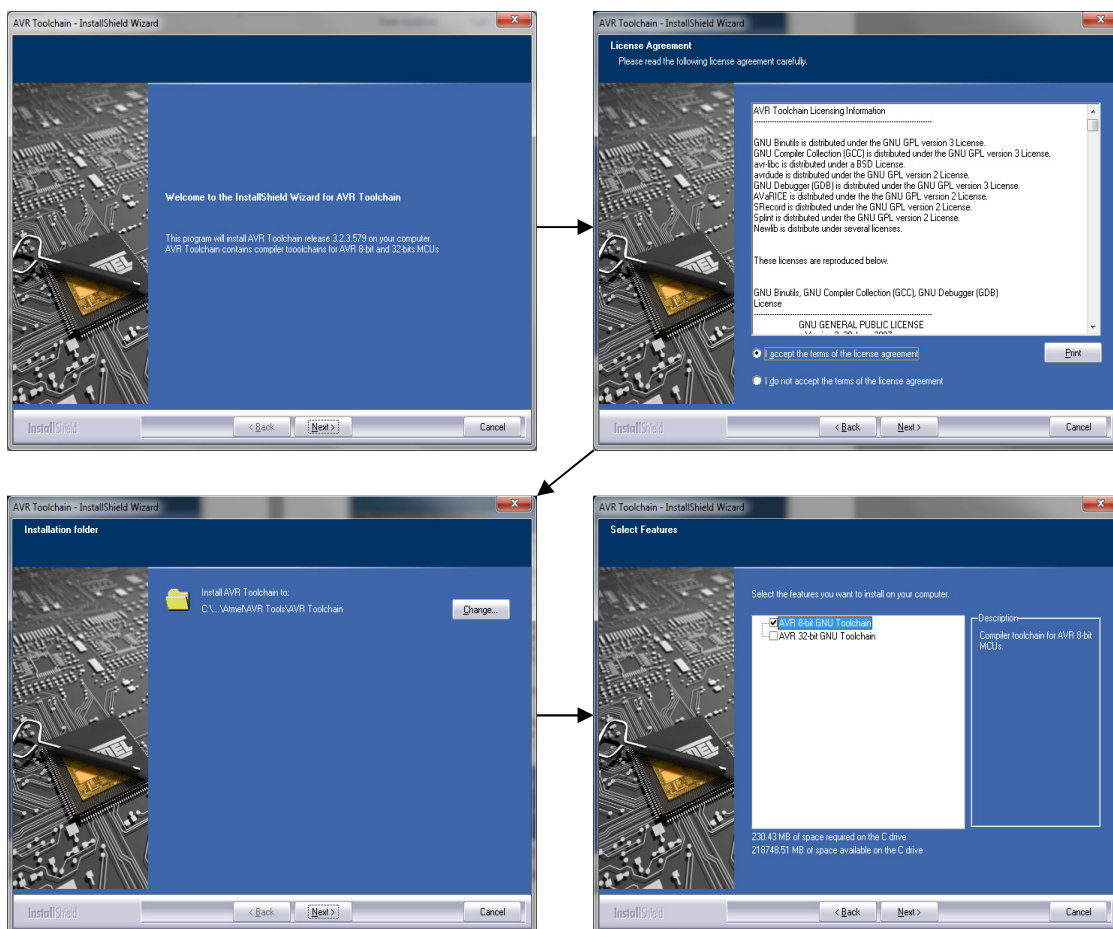
- Open the file AvrStudio4Setup.exe file with a right click and select Run As Administrator. Follow the next 4 dialogue boxes as shown.



- Proceed with the installation. This will install AVRStudio4 and the Jungo USB drivers for the JTAG debugger.

## 7.1.4 Installing the AVR GNU Compiler Tools.

- Once AVRStudio4 is installed open the file avr-toolchain-installer-3.3.0.710-win32.win32.x86.exe with a right click and select Run As Administrator. Follow the next 4 dialogue boxes as shown.



- In the last dialogue box select only the 8-bit tool chain for the Atmel AVR chip.

This will complete the installation of AVRStudio4 and the Atmel GCC tools.

## 7.2 Installing AVRStudio6

AVRStudio 6 is a new consolidated IDE and debugger developed by Atmel to support both their 8 bit and 32 bit microcontrollers. It uses the Microsoft Visual Studio IDE framework so may be familiar to some users.

Click on the as5installer-stable-5.1.208-full.exe (with Administrator rights if possible) and follow the installation instructions.

Both AVRStudio4 and AVRStudio 6 and the GCC tools can be installed at the same time without conflict. AVRStudio 5 will install it's own private copy of GCC that won't conflict with the separately installed v3.3.0.

AVRStudio 6 is relatively new and isn't as mature as the older but still very capable AVRStudio4.

## 7.3 JTAG Debuggers and ISP Programmers

The following JTAG debuggers are recommend for use with the ATX-PRO (connected to J7) and both AVRStudio4 and AVRStudio 6. They support code downloading, memory inspection and breakpoints.

ISP only programming is also available using the JTAG programmers on J9 as well as other ISP only devices. The ISP port uses the SPI protocol to read and write the all the memory spaces on an AVR chip. ISP is especially suited for programming the flash memory on the ATX-PRO for batch production in a factory. Development using the ISP port only is not recommended as it doesn't support breakpoints and code inspection.

Name	URL	Description
AVRDragon AVR JTAGICE mkII AVR ONE! JTAGICE 3	<a href="http://www.atmel.com">http://www.atmel.com</a>	JTAG Debugger and ISP Programmer. These programmers are officially supported by Atmel and the AVR Studio IDEs. The AVRDragon has been tested with AVRStudio 4 and 5 with the ATX-PRO.
JTAGICE mkII-CN	<a href="http://www.mcuzone.com">http://www.mcuzone.com</a>	JTAG Debugger and ISP Programmer. This is a 3 <sup>rd</sup> party JTAG debugger that is compatible with Atmel's JTAGICE mk-II and can be used for programming and debugging in AVRStudios 4 and 5. This has been tested with AVRStudio 4 and 5 and the ATX-PRO.
Arduino	<a href="http://www.arduino.cc">http://www.arduino.cc</a>	Serial Port Programmer The serial port on J6 and a standard RS232 cable are used to download and debug code using the Arduino IDE.
FTDI UM232H, C232HM and AVRDUDE	<a href="http://www.glyn.com.au">http://www.glyn.com.au</a>  AVRDUDE Software for UM232H: <a href="http://helix.air.net.au">http://helix.air.net.au</a>	ISP Only Programmer AVRDUDE is an open source utility designed to read and write the non volatile memories on Atmel AVR components. The FTDI UM232H module and C232HM cable supplied by Glyn can be used with an updated version of AVRDUDE.

Programming using the ISP port and a UM232H module with AVRDUDE has been tested with the ATX-PRO. In order for this to work download AVRDUDE from <http://helix.air.net.au>. Or the downloads section of <http://www.nongnu.org/avrdude/>. This binary version is currently only available for Windows.

The website <http://helix.air.net.au> has detailed instructions on using installing, connecting and using the UM232H and will be kept up to date over time.

It is expected that AVRDUDE v6 onwards will fully support the FTDI based parts and models in Windows, Linux and FreeBSD.



## 8 Installing the Arduino IDE

The ATX-PRO can also be programmed and driven using the popular Arduino suite. A slightly altered Arduino bootloader will need to be installed though - this will be covered below. To install the Arduino programming environment follow the instructions at:

<http://arduino.cc/en/Guide/HomePage>.

The ATX-PRO has been tested with Arduino version 1.0. Glyn can preload the modified bootloader if required before shipping.

All that is required to develop with the Arduino IDE and the ATX-PRO is a standard RS232 cable (native or USB based) connected to J6.

### 8.1 Alternative Arduino Bootloader

The Arduino bootloader code expects to communicate with the host computer at 56700 baud. The default Arduino bootloader for the Atmega1280 is configured for the Arduino Mega board and expects that the system clock runs at 16MHz. As the ATX-PRO operates at 11.0592MHz the serial port speeds will be wrong using the default image file from Arduino.

To build the corrected bootloader the following prerequisites of Arduino 1.0 and the AVR GNU Compiler in section 1.4.

- Open the Makefile in a text editor in the path:

```
<INSTALLPATH>\arduino-1.0\hardware\arduino\bootloaders\atmega\Makefile
```

```
ATX-PRO: TARGET = ATX-PRO
ATX-PRO: MCU_TARGET = atmega1280
ATX-PRO: CFLAGS += '-DMAX_TIME_COUNT=F_CPU>>4' '-DNUM_LED_FLASHES=0' -DBAUD_RATE=57600
ATX-PRO: AVR_FREQ = 11059200L
ATX-PRO: LDSECTION = --section-start=.text=0x1F000
ATX-PRO: $(PROGRAM)_ATX-PRO.hex
```

- Add the following at line 191 then save the Makefile:

If the GCC tools are installed correctly type in to a command line in the same directory as the makefile:

```
make ATX-PRO
```

The new hex file called ATmegaBOOT\_168\_ATX-PRO.hex will be generated and can be installed via JTAG or the ISP port. Once this new version is generated and installed it will accept code downloads from the Arduino IDE.

### 8.2 Adding a New Board to the Arduino IDE

A board configuration can be added to the Arduino IDE so that it appears in the menu Tools->Board->Glyn ATX-PRO.

- Open the boards.txt file in a text editor in the path:

```
<INSTALLPATH>\arduino-1.0\hardware\arduino\boards.txt
```

- Add the following (cut and paste) at line 1 then save the file:

```

ATX-PRO.name=Glyn ATX-PRO

ATX-PRO.upload.protocol=arduino
ATX-PRO.upload.maximum_size=126976
ATX-PRO.upload.speed=57600

ATX-PRO.bootloader.low_fuses=0xFF
ATX-PRO.bootloader.high_fuses=0xDA
ATX-PRO.bootloader.extended_fuses=0xF5
ATX-PRO.bootloader.path=atmega
ATX-PRO.bootloader.file=ATmegaBOOT_168_ATX-PRO.hex
ATX-PRO.bootloader.unlock_bits=0x3F
ATX-PRO.bootloader.lock_bits=0x0F

ATX-PRO.build.mcu=atmega1280
ATX-PRO.build.f_cpu=11059200L
ATX-PRO.build.core=arduino
ATX-PRO.build.variant=mega

#####

```

## 9 Operating Systems

The ATX-PRO has been tested and operated with the following operating systems:

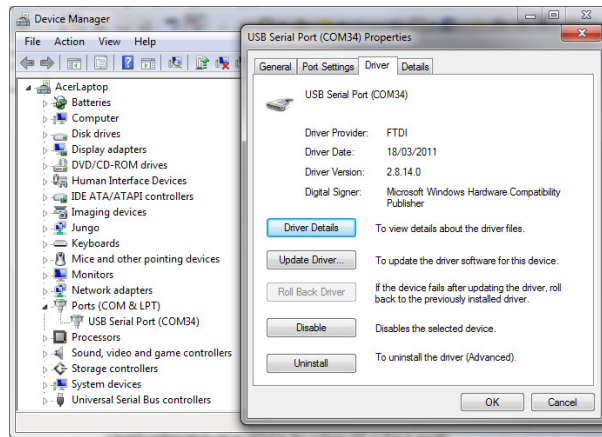
Name	URL	Description
FreeRTOS	<a href="http://www.freertos.org">http://www.freertos.org</a>	This is a popular and well tested RTOS with many powerful features for creating a robust embedded system. Examples exercising the ATX-PRO are available upon request from Glyn using AVRStudio 6.
BeRTOS	<a href="http://www.bertos.org">http://www.bertos.org</a>	This is a modular pre-emptive kernel with many peripheral drivers and utility functions. The system driver model is highly abstracted. This has been successfully compiled and debugged using AVRStudio4.
Arduino	<a href="http://www.arduino.cc">http://www.arduino.cc</a>	Arduino is a well known development system for AVR chips. A lot of the complexity of programming the chip is hidden at the cost of limited debugging. Source code and examples exercising the ATX-PRO specific functions are available upon request from Glyn.
MK RTOS	N/A	This is a simple scheduler and includes some timers and serial drivers. The source code and examples exercising the specific functions of the ATX-PRO are available upon request from Glyn. This has been successfully compiled and debugged using AVRStudio4.

## 10 Batch Programming with the FTDI C232HM

Glyn can supply the FTDI C232HM DDHSL-0 SPI/ISP programming cable for either low cost development or rapid batch programming for the factory or in field. This is used in conjunction with Windows and a free program called AVRDUDE to quickly read, write and verify the non-volatile memories in the ATmega1280.

### 10.1 Installation of the C232HM

On Windows Vista and Windows 7 plugging in the C232HM will cause Windows to automatically seek an FTDI driver from Microsoft. Once installed it will show up in the devices tree as follows:

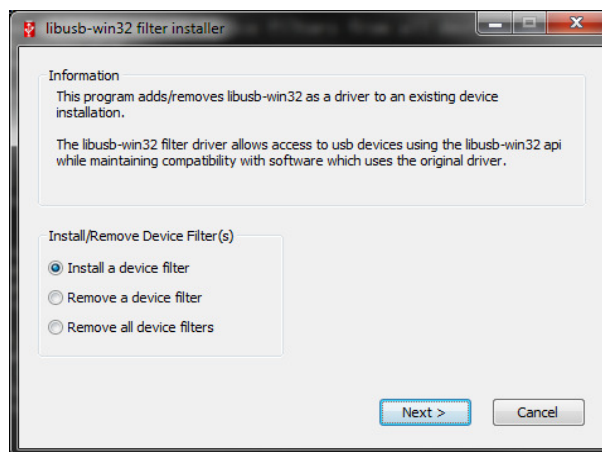


AVRDUDE requires the installation of the open source libusb driver in order to work with the FTDI chip. AVRDUDE uses the high speed SPI mode of the FTDI-232H chip in order to rapidly write and verify the flash memory on the AVR chip, it is no a so called bit-banger. To install the libusb driver go from:

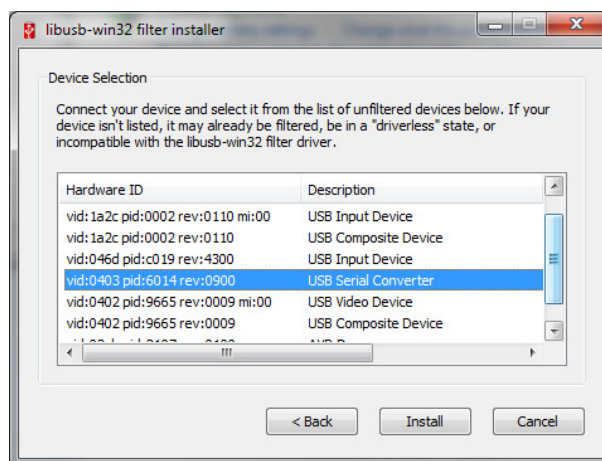
<http://sourceforge.net/projects/libusb-win32/files/libusb-win32-releases/1.2.6.0/libusb-win32-devel-filter-1.2.6.0.exe/download>

This driver is for all versions of Windows from XP to Windows 7 and will work with 32 and 64 bit systems.

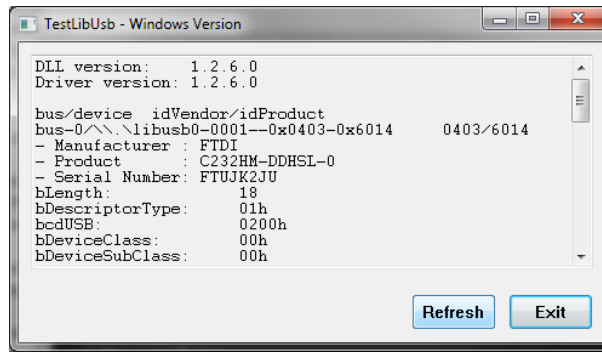
Once downloaded install the executable. The Start Menu should have a new entry called LibUSB-Win32. From that menu item run Filter Wizard which will bring up the follow screen:



Select Install device filter. Make sure that the C232HM is the only FTDI device plugged in.



Select the device with VID: 0403 and PID:6014 rev:0900 USB Serial Converter. This should be the C232HM. Select Install.



Once installed run the “Test (Win) Program” to check that it has installed. The above picture shows an example of a successfully installed filter driver. In the Windows device manager there should be no change to the state of the C232HM serial port and any Windows based applications that use FTDI’s device drivers should still work.

## 10.2 Installation of AVRDUDE

A version of AVRDUDE that will work with the C232HM is [avrdude-5.11svn1068-Patch7729-win32.zip](#). This is available from Glyn and new versions will be downloadable from <http://helix.air.net.au>.

The AVR Toolchain typically installs the older version 5.10 of AVRDUDE in:

C:\Program Files (x86)\Atmel\AVR Tools\AVR Toolchain\bin

Back up the files `avrdude.exe` and `avrdude.conf` in this directory and replace them with the files in the zip archive. This will make sure that whenever you run `avrdude` that the correct version will be executed. Once installed open up a command window and type in “`avrdude -v`” and the response should be as follow:

```
avrdude: Version 5.11svn1068-patch7729, compiled on Feb 25 2012 at 22:00:35
```

## 10.3 Using AVRDUDE and the C232HM.

The ISP header (J9) on the ATX-PRO and cable on the C232HM should be connected as follows:



Pin	Colour	Net Name	I/O	Description
1	Green	MISO	O	Master In Slave Out
2	N/C	3V3	O	ISP Sense (no connection)
3	Orange	SCK	I	ISP Clock
4	Yellow	MOSI	I	Master Out Slave In
5	Brown	RESET	I	Reset
6	Black	GND		System ground

To program in a hex file generated by AVRStudio the following command should be invoked.

```
avrdude -c c232hm -p m1280 -b 2500000 -U flash:w:ATmegaBOOT_168_ATX-PRO.hex
```

The invocation arguments are as follows:

-c: The programmer type. This is defined in the `avrdude.conf` file.

-p: The chip type. The ATX-PRO uses the `Atmega1280`.

-b: The SPI bit rate. This is  $\frac{1}{4}$  or less of the CPU clock speed. For an 11MHz ATX-PRO 2500000Hz works reliably.

-U: The memory region (flash), the operation (w for write) and the hex file name.

The output from AVRDUDE for the above command is as follows:

```
avrdude: AVR device initialized and ready to accept instructions

Reading | ##### | 100% 0.04s

avrdude: Device signature = 0x1e9703
avrdude: NOTE: FLASH memory has been specified, an erase cycle will be performed
        To disable this feature, specify the -D option.
avrdude: erasing chip
avrdude: reading input file "ATmegaBOOT_168_ATX-PRO.hex"
avrdude: input file ATmegaBOOT_168_ATX-PRO.hex auto detected as Intel Hex
avrdude: writing flash (129406 bytes):

Writing | ##### | 100% 1.70s

avrdude: 129406 bytes of flash written
avrdude: verifying flash memory against ATmegaBOOT_168_ATX-PRO.hex:
avrdude: load data flash data from input file ATmegaBOOT_168_ATX-PRO.hex:
avrdude: input file ATmegaBOOT_168_ATX-PRO.hex auto detected as Intel Hex
avrdude: input file ATmegaBOOT_168_ATX-PRO.hex contains 129406 bytes
avrdude: reading on-chip flash data:

Reading | ##### | 100% 1.74s

avrdude: verifying ...
avrdude: 129406 bytes of flash verified

avrdude: safemode: Fuses OK

avrdude done. Thank you.
```

The complete AVRDUDE manual is available at <http://www.nongnu.org/avrdude/user-manual/avrdude.html>.

## 11 Getting Started Guide